Practical RTL Verification

Introduction:

RTL verification is one of the crucial stages and almost 60% of the time is spent on functional verification of the RTL design concerned in a standard ASIC design flow. This means that there is a huge requirement of human resources skilled in this domain. In this course, we will cover the complete verification flow and explore various techniques using Verilog, Systemverilog and UVM for RTL Verification.

Objectives:

By the end of this course, you should be able to:

1. Explain the verification flow
2. Analyze the design specifications and build a verification plan
3. Write test benches using Verilog HDL and Systemverilog HVL
4. Use UVM for building sophisticated test benches for IPs
5. Write appropriate test cases for the design under test
6. Understand coverage and achieve coverage goals for a given verification activity
7. Understand the importance of assertions and use them efficiently in test benches
8. Employ FPGAs for verification of RTL designs

Pre-requisites:

1. Digital logic
2. Knowledge of VHDL and /or Verilog HDL is desirable

Who should attend?

This course is meant for graduate, post-graduate students and fresh engineers who wish to develop their skill set in verification methodologies. It is beneficial for corporate people who wish to enhance their skill set for better opportunities.

Contents:

Stage 1:

1. Verification fundamentals and verification flow
2. Verilog HDL review
3. Writing automatic test benches in Verilog
4. Mini-project

Stage 2:

Systemverilog for RTL Verification

1. Language constructs
2. Arrays and queues
3. Tasks and functions
4. Mailboxes and semaphores
5. Interfaces and clocking blocks
6. OOP constructs
7. Randomization
8. Coverage constructs
9. Fundamentals of assertions
10. Mini-project (Wishbone IP)

Stage 3:

UVM

1. Overview of UVM
2. Reporting in UVM
3. TLM
4. UVM Factory
5. Configurations
6. Analysis components
7. Connecting the DUT
8. Stimulus generation
9. Configurations
10. Introduction to UVM registers
11. Mini-project (APB IP)

Stage 4:

Using FPGAs for Verification

Stage 5:

Project work: (AXI IP)

Cost:

Rs. 25000/-

Please contact us for discounts for multiple participants.

Mode of delivery:

1. Class-room sessions
2. Online